Obtaining the High-resolution Epoch with the FPGA Technology

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Abstract

In Satellite Laser Ranging it is important to record the transmission epoch of each laser pulse. Currently in the Beijing SLR station many counter-chips are used to accomplish this task. With the popularity of the FPGA technology, engineers find that using FPGA (Field Programmable Gate Array) to design the digital system is a feasible way to reduce the dimension of the circuit board and increase the reliability of the system. We are designing a new epoch measurement system using one Xilinx's Spartan FPGA chip to accomplish what previously had required many counter-chips. The 1pps signals and the time code from the HP58503 are used to get rough epoch information to a one second resolution. The 10 MHz frequency from the HP58503 is used as the system clock. A 24-bit counter module in the FPGA chip, used with the system clock, gives timing information with a resolution of 100 nanoseconds and with a period of one second. To obtain the time code from the HP58503, two UART (Universal Asynchronous Receiver) modules are used, one to communicate with the HP58503, and another to transfer the epoch data to a PC.

Introduction

Fig.1 shows the present module at the Beijing Station that is used to obtain the epoch of the laser pulse. It is the cascade connection of 6 counter-chips. Every chip is only 4 bits, so higher resolution requires more counter-chips. To achieve a higher integrated level, we selected the FPGA chip which would perform the same task in a single module.

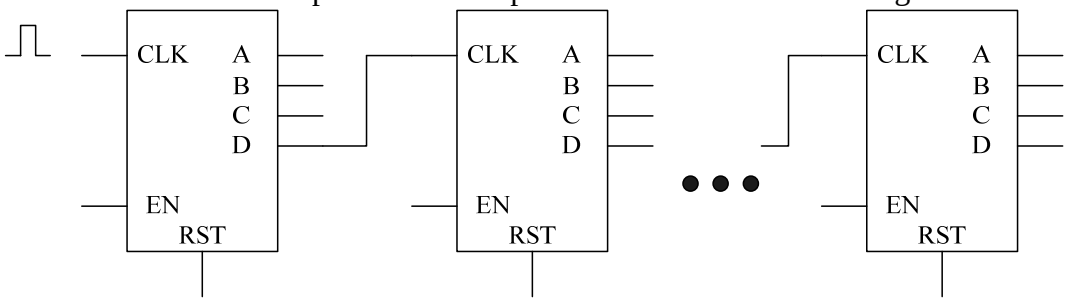

Figure 1: *Present module to obtain the epoch in Beijing Station*

Fig.2 shows the block scheme of the system. The HP58503 supplies the reference frequency, the one-pulse-per-second signal and the time code for the FPGA module to establish a UTC time clock. When a laser pulse arrives, the FPGA module sends the epoch data to the PC through the Serial Interface. MAX3232 is used as the level translator between the RS232 and LVTTL.

Establishment of the UTC time clock

Fig.3 shows the block scheme of the establishment of the UTC time clock. As the input clock frequency is 10MHz, so the time resolution is 100ns. To record one complete second, we must use a counter with at least 24 bits, because,

$$\log_2 \frac{1}{100 \times 10^{-9}} = 23.3$$

It’s convenient to design a 24-bit counter in FPGA. Another 16-bit counter is designed to record the number of 1pps events after the reset operation. The 16-bit counter can record the time up to 18 hours, so 18 hours later, another reset operation is needed. Some registers are used to record the time code from the HP58503 to save the datum time.

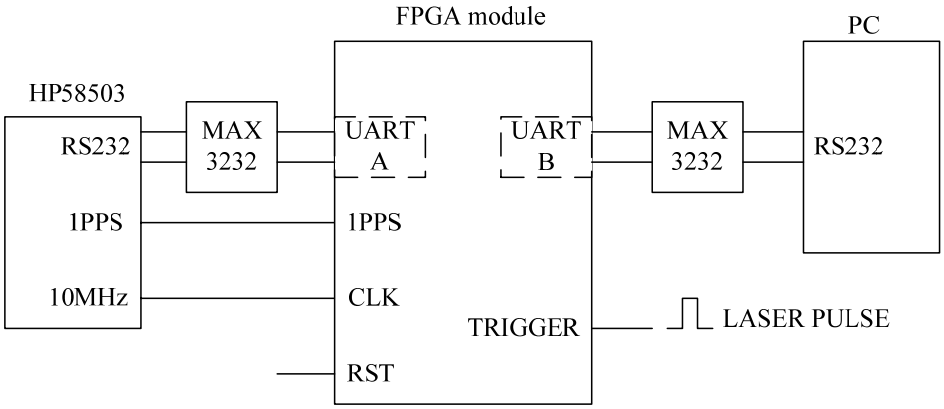

Figure 2: *Block scheme of the system*

Obtaining the epoch of the laser pulse

When a laser pulse arrives, some relative-time-registers are allocated to store the current values of REG1 and REG2. Then the data in the datum-time-registers and relative-time-registers are sent to the PC through UART B. The PC performs the final calculations required to obtain the transmission epoch of the laser pulse.

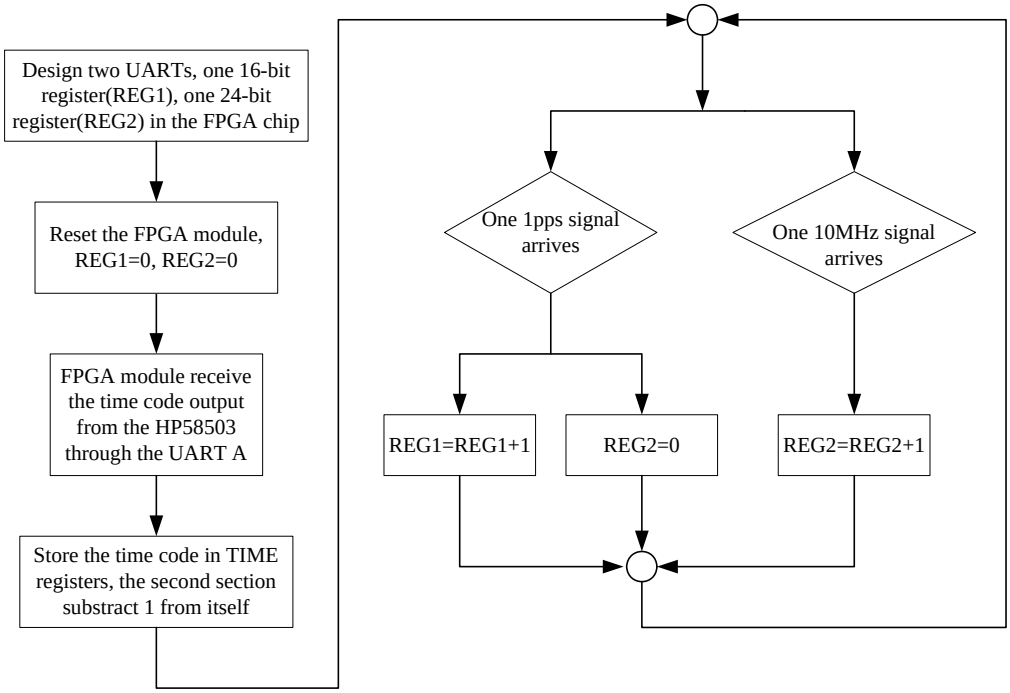

Figure 3*: The Establishment of the UTC time clock*

Comparison experiment and conclusion

A test setup has been designed to make sure that the new module can obtain the time code, 10MHz signal, 1pps signal from HP58503 as well as the laser pulse without disturbing the original system. Comparing the two epoch data shows that the new module has the equivalent function to the original one.

Difficulties in the development process and Future Plans

In the development process, the implementation of the UART is relatively harder than that of the counters. So compared with the microprocessors, the merits and drawbacks of developing a digital system with an FPGA are obvious.

Today, RISC microprocessors with an ARM core are widely used to design digital systems, so the structure “ARM+FPGA” may be a good choice for developing a digital system that can achieve higher resolution, precision, stability, flexibility and integration level as well as shorten the development time.

Platform

- Device:

  - Xilinx’s Spartan FPGA, HP58503, PC

- Software:

  - Xilinx ISE 7.1

  - VC++ 6.0

- Top-level Module type

  - HDL(Verilog HDL)

- Simulator

  - ISE Simulator

- Synthesis

  - XST(VHDL/verilog)